DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirawa (6831674 B2) in view of Hata (6201451 B1).

Regarding claim 1, Hirawa discloses, in figures 5 and 8, spatial light modulator, comprising: memory elements (431) configured to store data (512) therein and shift data (512) therebetween (col. 7, lines 1-3); and light modulation elements (121) respectively in communication with the memory elements (431) (col. 7, lines 3-4), wherein each of the light modulation elements (121) is alterable in response to data (512) stored in the respectively corresponding memory elements (431) (col. 7, lines 3-4 and 7-9) but does not specifically disclose wherein said memory elements are configured to shift the data bi-directionally. Hata discloses wherein said memory elements are configured to shift the data bi-directionally (col. 7, lines 66-67 and col. 8, lines 1-6). Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to combine the device of Hirawa with the bi-direction shift of Hata for the purpose of depending on the binary logic, the data shifts in one direction if the shift pulse indicates "1" and another direction if the shift pulse indicates “0” (col. 7, lines 66-67 and col. 8, lines 1-6).

Regarding claim 7, Hirawa discloses the claimed invention but does not specifically disclose wherein said memory elements are static memory elements. It would have been obvious to one having ordinary skill in the art at the time of the invention to modify the invention to include static memory elements for the purpose of the memory elements maintaining a constant position.

Regarding claims 8 and 9, Hirawa discloses, in figures 5 and 8, spatial light modulator, wherein each of the memory elements (431) includes a feedback element (col. 7, lines 1-9).

3. Claims 2-6, 10, and 12-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirawa (6831674 B2) in view of Hata (6201451 B1) as applied to claim 1 above, and further in view of Moore et al. (2003/0096497 A1).

Regarding claim 2, Hirawa and Hata disclose the claimed invention but does not specifically disclose wherein said memory elements are arranged in an array having rows and columns. Moore et al. discloses, in figure 4, wherein said memory elements (402) are arranged in an array having rows and columns (section 0036, lines 2-3). Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to combine the device of Hirawa with the rows and columns of Moore et al. for the purpose of transferring data between the array of elements (section 0036).

Regarding claim 3, Hirawa and Hata disclose the claimed invention but does not specifically disclose wherein said memory elements are configured to shift the data bi-directionally between rows. Hata discloses wherein said memory elements are configured to shift the data bi-directionally between rows (col. 7, lines 66-67 and col. 8, lines 1-6). Therefore

it would have been obvious to one having ordinary skill in the art at the time of the invention to combine the device of Hirawa with the bi-direction shift of Hata for the purpose of depending on the binary logic, the data shifts in one direction if the shift pulse indicates "1" and another direction if the shift pulse indicates "0" (col. 7, lines 66-67 and col. 8, lines 1-6).

Regarding claim 4, Hirawa and Hata disclose the claimed invention but does not specifically disclose wherein said memory elements are configured to shift the data bi-directionally between columns. Hata discloses wherein said memory elements are configured to shift the data bi-directionally between columns (col. 7, lines 66-67 and col. 8, lines 1-6). Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to combine the device of Hirawa with the bi-direction shift of Hata for the purpose of depending on the binary logic, the data shifts in one direction if the shift pulse indicates "1" and another direction if the shift pulse indicates "0" (col. 7, lines 66-67 and col. 8, lines 1-6).

Regarding claim 5, Hirawa and Hata disclose the claimed invention but does not specifically disclose wherein said memory elements are configured to shift the data bi-directionally between at least one of non-adjacent rows and non-adjacent columns. Hata discloses wherein said memory elements are configured to shift the data bi-directionally between at least one of non-adjacent rows and non-adjacent columns (col. 7, lines 66-67 and col. 8, lines 1-6). Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to combine the device of Hirawa with the bi-direction shift of Hata for the purpose of depending on the binary logic, the data shifts in one direction if the shift pulse indicates "1" and another direction if the shift pulse indicates "0" (col. 7, lines 66-67 and col. 8, lines 1-6).

Regarding claim 6, Hirawa and Hata disclose the claimed invention but does not specifically disclose wherein said memory elements are arranged in a non-orthogonal pattern. Moore et al. discloses, in figure 4, wherein said memory elements are arranged in an orthogonal pattern. However, it would have been obvious to one having ordinary skill in the art at the time of the invention to modify the invention to include memory elements are arranged in a non-orthogonal pattern for the purpose of transferring data in various patterns and directions.

Regarding claim 10, Hirawa and Hata disclose the claimed invention but does not specifically disclose access control elements connected to said respective memory elements. Moore et al. discloses, in figure 4, access control elements (404) connected to said respective memory elements (403) (section 0036, lines 2-8). Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to combine the device of Hirawa with the access control elements of Moore et al. for the purpose of controlling the operation of the memory elements (section 0036, lines 2-8).

Regarding claim 12, Hirawa and Hata disclose the claimed invention but does not specifically disclose wherein each of said memory elements further includes an output node electrically coupled to an electrode of said respective light modulation element and to an input node of an additional one of said memory elements. Moore et al. discloses, in figure 4, wherein each of said memory elements (402) further includes an output node electrically coupled to an electrode (406) of said respective light modulation element (402) and to an input node of an additional one of said memory elements (402) (section 0036).

Regarding claim 13, Hirawa discloses, in figures 5 and 8, spatial light modulator, wherein said memory elements (431) are interconnected in a shift register configuration (col. 7, lines 1-3).

Regarding claim 14, Hirawa, Hata, and Moore et al. disclose the claimed invention but does not specifically disclose wherein said memory elements each include a master-slave flip-flop. It would have been obvious to one having ordinary skill in the art at the time of the invention to modify the invention to include wherein said memory elements each include a master-slave flip-flop for the purpose of two gated D latches in series, and invert the enable input to one of them.

Regarding claim 15, Hirawa discloses, in figures 5 and 8, spatial light modulator, further comprising: a timing circuit (521) in communication with each of said memory elements (431) to shift the data between said memory elements (431) (col. 7, lines 1-3).

Regarding claim 16, Hirawa discloses, in figures 5 and 8, spatial light modulator, wherein said timing circuit 9521) is a ripple clock (col. 7, lines 1-3).

Regarding claim 17, Hirawa, Hata, and Moore et al. disclose the claimed invention but does not specifically disclose wherein said light modulation elements comprise liquid crystal material. It would have been obvious to modify the invention to include liquid crystal material, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use (In re Leshin, 125 USPQ 416). Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention to include wherein the light modulation elements comprising liquid crystal material for the purpose of using a lithography system.

1. Claims 18, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirawa (6831674 B2) in view of Hata (6201451 B1) in view of Moore et al. (2003/0096497 A1).as applied to claim 1 above, and further in view of Bhuva et al. (5612713).

Regarding claim 18, Hirawa, Hata, and Moore et al. discloses the claimed invention but does not specifically disclose wherein said light modulation elements further comprise: a common electrode configured to receive a common electrode signal for said light modulation elements; and a respective pixel electrode configured to receive the data stored in said respective memory elements. Bhuva et al. discloses, in figures 2 and 3, a spatial light modulator, wherein said light modulation elements (10) further comprise: a common electrode (15) configured to receive a common electrode signal for said light modulation element s (10) (col. 3, lines 28-30); and a respective pixel electrode (14) configured to receive the data stored in said respective memory elements (10) (col. 3, lines 31-34). Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to combine the device of Hirawa and Moore et al. with the electrodes of Bhuva et al. for the purpose of receiving the data from the memory elements (col. 3, lines 31-34).

Regarding claim 20, Hirawa, Hata, and Moore et al. discloses the claimed invention but does not specifically disclose wherein said light modulation elements comprise micromirrors. Bhuva et al. discloses, in figures 2 and 3, a spatial light modulator, wherein said light modulation elements (10) comprise micromirrors (21) (col. 3, line 66). Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to combine the device

of Hirawa and Moore et al. with light modulation elements of Bhuva for the purpose of reflecting light.

Regarding claim 21, Hirawa, Hata, and Moore et al. discloses the claimed invention but does not specifically disclose wherein said memory elements are arranged in blocks, a first one of said blocks configured to receive data from an external input and the others of said blocks configured to receive data from other ones of said memory elements. Bhuva et al. discloses, in figures 2 and 3, a spatial light modulator, wherein said memory elements (10a) are arranged in blocks (31) (col. 4, lines 53-55), a first one of said blocks (31) configured to receive data from an external input and the others of said blocks configured to receive data from other ones of said memory elements (10a) (figure 3). Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to combine the device of Hirawa and Moore et al. with the memory elements of Bhuva et al. for the purpose of inputting and outputting data (col. 4, lines 53-55).

2. Claims 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gale et al. (5285407) in view of Hirawa (6831674 B2)

Regarding claims 22 and 25, Gale et al. discloses, in figures 2A, 2B, and 3, a method for performing photolithography, said method comprising: altering ones of the light modulation elements (21) in response to the data loaded thereunto to transfer the image onto a substrate (col. 5, lines 9-12); shifting the data between memory elements (col. 4, lines 7-11, 17-24); altering ones of the light modulation elements (21) in response to the data shifted thereunto to transfer the image onto the substrate (col. 4, lines 7-11, 17-24) but does not specifically disclose loading data

representing an image into memory elements in communication with respective light modulation elements. Hirawa discloses light modulation elements (121) respectively in communication with the memory elements (431) (col. 7, lines 3-4). Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the device of Gale with the modulation elements of Hirawa for the purpose of displaying the stored and shifted data (col. 7, lines 3-4).

Regarding claim 23, Gale et al. discloses, in figures 2A, 2B, and 3, a method for performing photolithography, wherein each said altering further comprises: applying a voltage in response to the data to the change optical characteristics of the light modulation elements (21) (col. 4, lines 44-61).

Regarding claim 24, Gale et al. discloses, in figures 2A, 2B, and 3, a method for performing photolithography, wherein said shifting further comprises: utilizing a ripple clock to control the timing of said shifting (col. 4, lines 13-16).

Regarding claim 26, Gale et al. discloses, in figures 2A, 2B, and 3, a method for performing photolithography, wherein said altering in response to the shifted data is performed after said moving (col. 5, lines 9-12).

Allowable Subject Matter

3. Claims 11 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art taken either singularly or in combination fails to anticipate or fairly suggest the limitations of the independent claim(s), in such a manner that a rejection under 35 U.S.C. 102 or 103 would be proper. The prior art fails to teach a combination of all the claimed features as presented in claim(s) 11 and 19, wherein the claimed invention comprises, in claim 11, access control elements including a forward access control element and a reverse access control element; in claim 19, a timing circuit that shifts inverted data from a first to a second memory element and switches the common electrode signal, as claimed.

Response to Arguments

4. Applicant's arguments with respect to claims 1-26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BRANDI N. THOMAS whose telephone number is (571)272-2341. The examiner can normally be reached on Monday - Thursday from 6-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Mack can be reached on 571-272-2333. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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BNT
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